#3

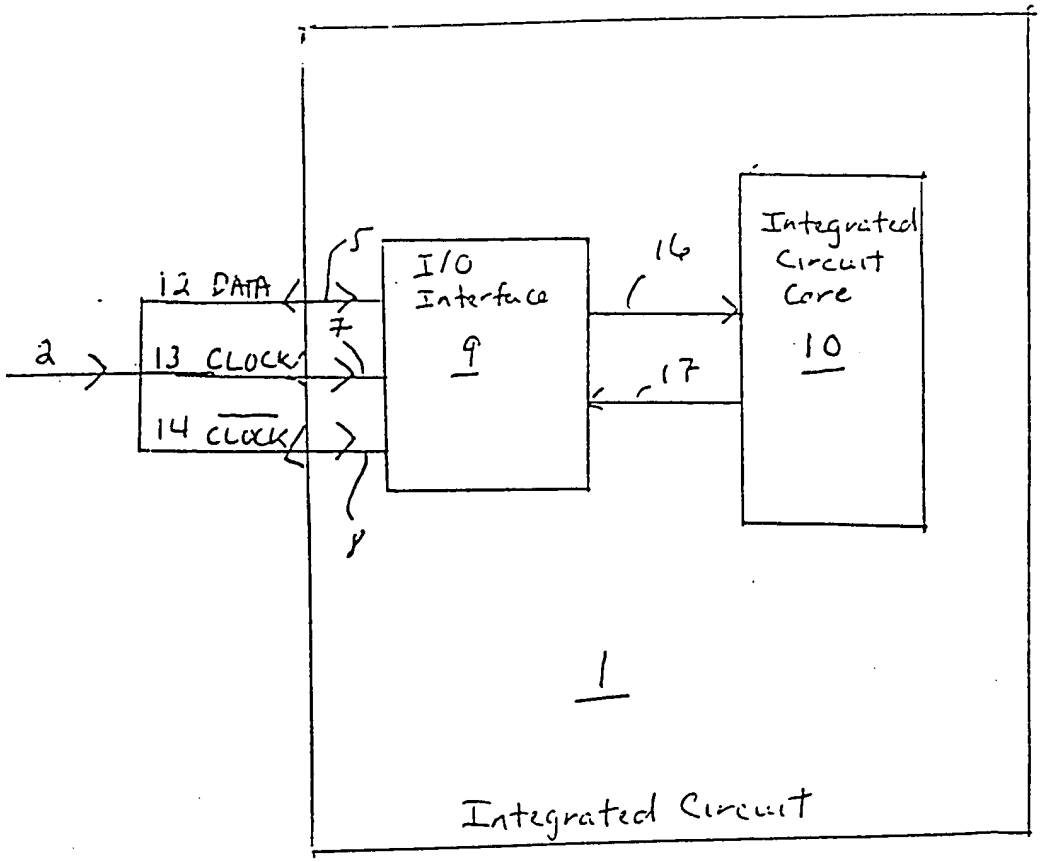

12 DATA
13 CLOCK
14 $\overline{\text{CLOCK}}$
2
5
7
9
I/O Interface
16
17
Integrated Circuit Core
10
1
Integrated Circuit

FIG. 1

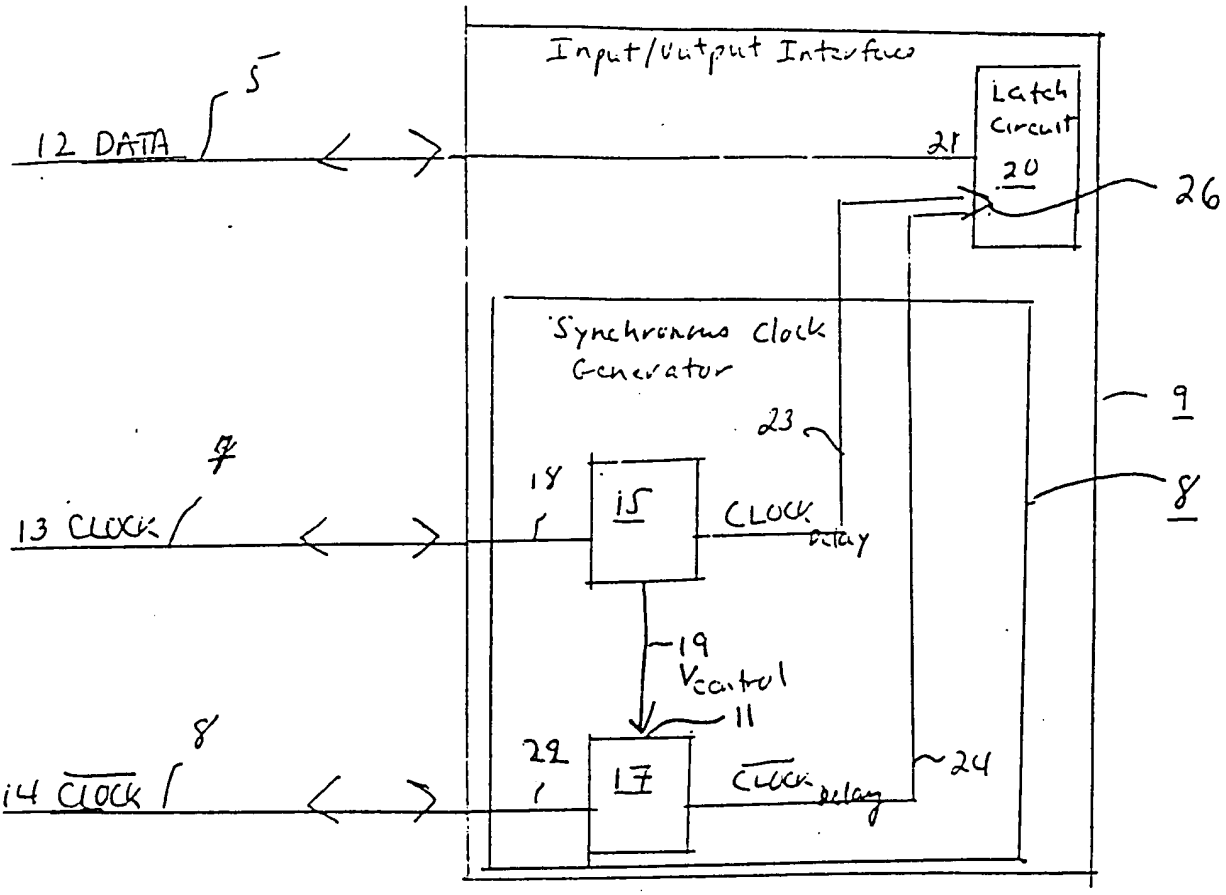

Input/Output Interface
Latch Circuit
20
21
26
12 DATA
5
Synchronous Clock Generator
9
23
8
13 CLOCK
7
18
15
CLOCK Delay
19
Vcontrol
11
14 CLOCK
8
22
17
CLOCK delay
24

FIG. 2

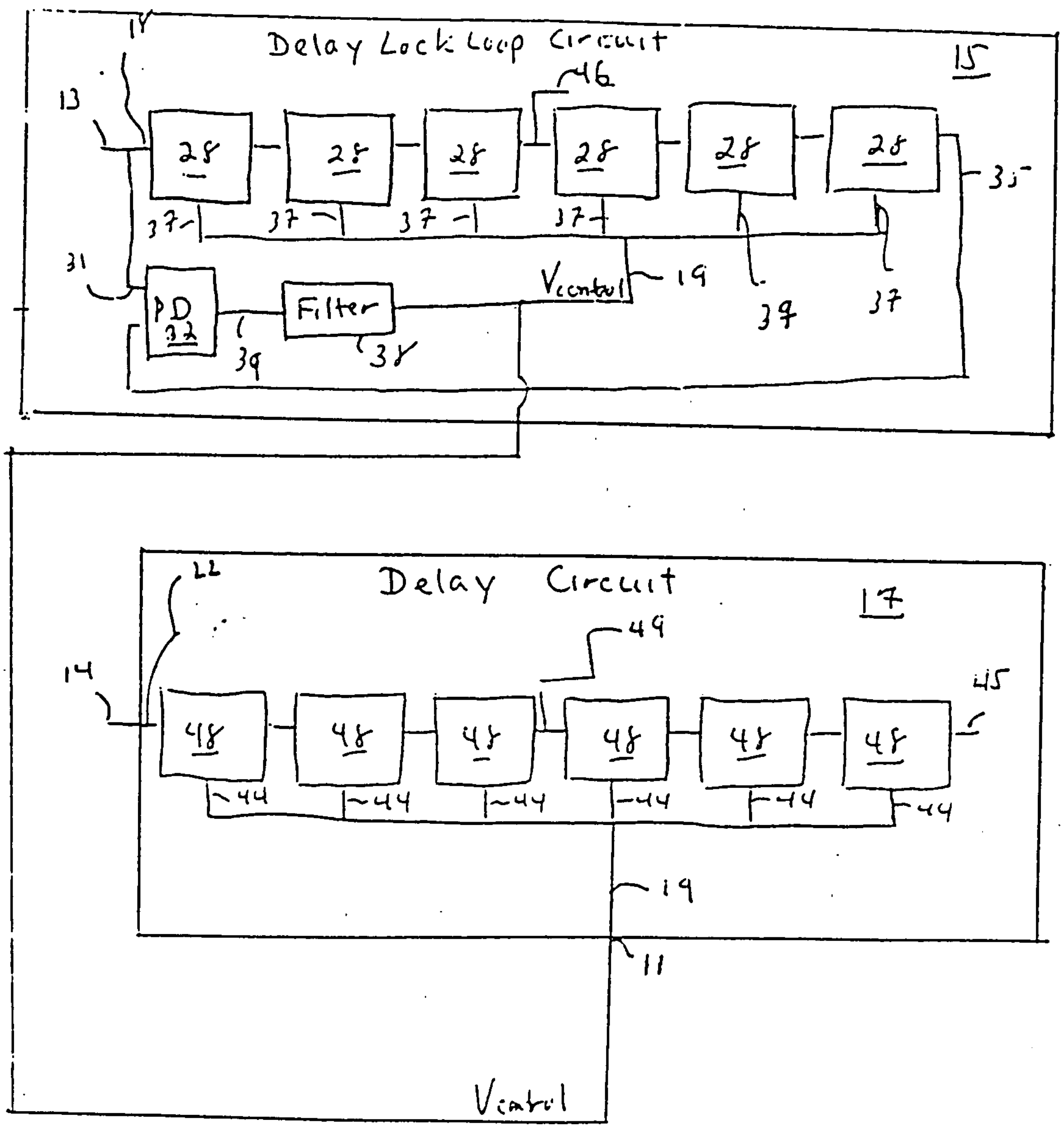
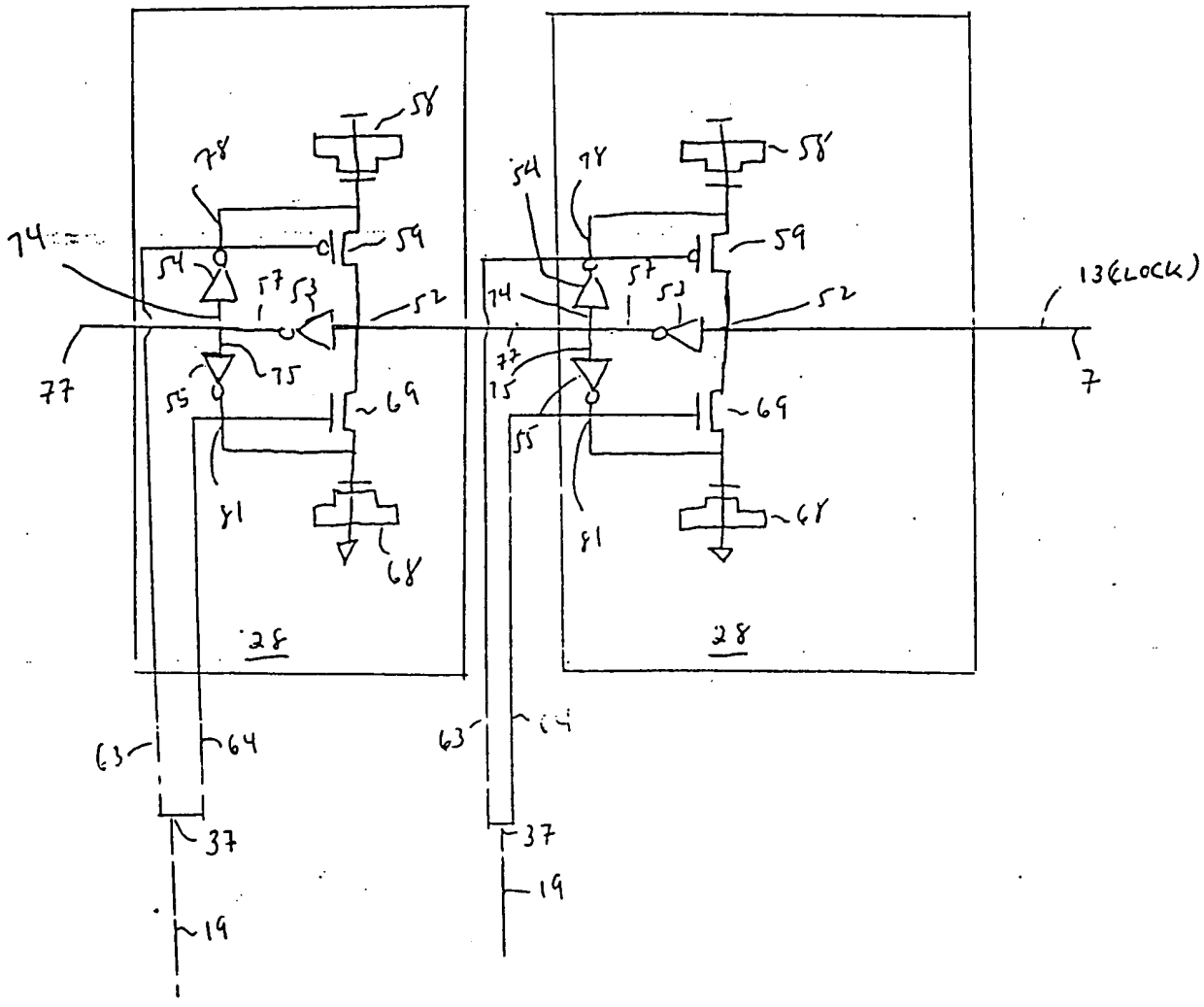


FIG. 3

FIG. 4



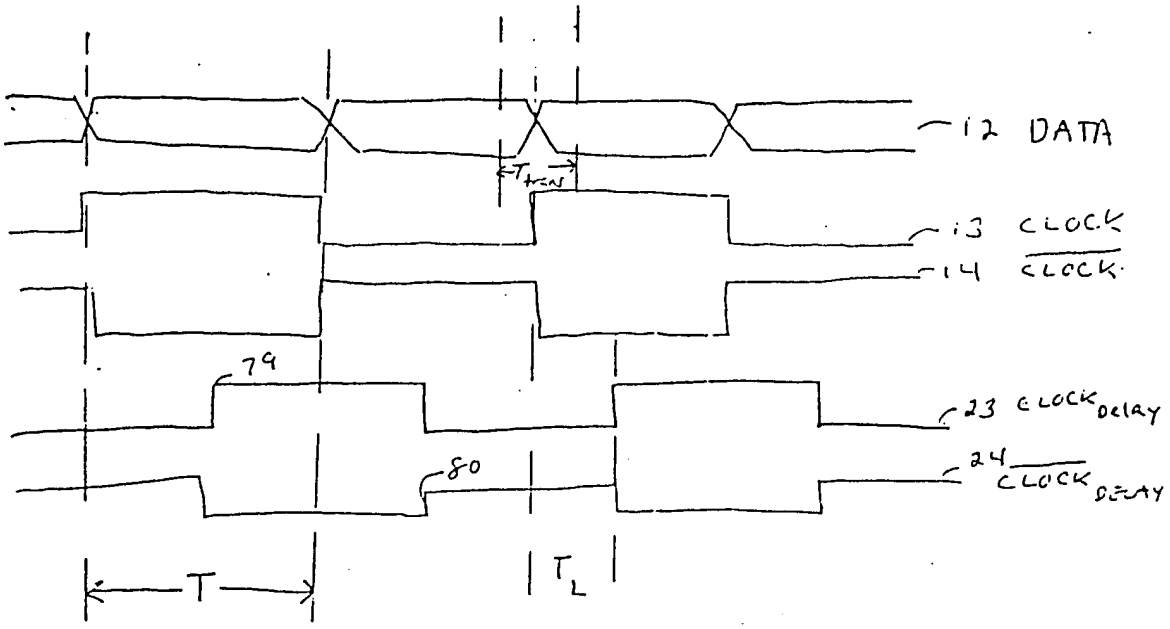

12 DATA
T_{trans}
13 CLOCK
14 $\overline{\text{CLOCK}}$
79
23 $\text{CLOCK}_{\text{DELAY}}$
80
24 $\overline{\text{CLOCK}}_{\text{DELAY}}$
T
T_L

FIG. 5